CompactPCI Hot Swap Controller with I²C Interface, Bus Precharge and On-Chip LOCAL_PCI_RESET# Logic

by Victor Fleury

Introduction

When a board is plugged into the live backplane of a host system (hot swapped), the bulk bypass capacitors of the board can draw large inrush currents as they charge. These transient currents can damage connectors or create glitches on the backplane, potentially causing other boards in the system to inadvertently reset. To prevent such large inrush currents, the bulk bypass capacitors on the plug-in board must be isolated during the Hot Swap sequence.

The LTC4240 provides a controlled on-off switch for four hot swappable board power supply voltages, allowing the board to be safely inserted or removed from a live CompactPCI (CPCI) slot without disturbing the system power supplies. The LTC4240 includes an I²C-compatible interface that allows software control and monitoring of device function and power supply status.

Hot Swap features include:

- ❑ PRECHARGE output for biasing I/O connector pins during board insertion and extraction
- ❑ Circuit breakers on all four supplies with 35µs overcurrent glitch filters
- ❑ Foldback current limit to reduce power dissipation while charging large capacitive loads and during short circuit conditions
- ❑ Supports backplanes with and without bypass capacitors

I²C read and write functions include:

- ❑ Under a fault condition, determine which supply created the fault
- ❑ Read the maximum allowed board power consumption: PRSNT1#, PRSNT2#
- ❑ Cycle board power, reset the board after a fault condition
- ❑ Ignore faults on the +12V and –12V supplies

Typical Hot Swap Application

Figure 1 shows a CPCI Hot Swap application. Transistors Q1 and Q2 isolate 3.3V and 5V backplane power supplies from the plug-in board's bulk capacitance. The currents through Q1 and Q2 are sensed by R1 and R2. Resistors R3 and R4 prevent high frequency oscillations in Q1 and Q2. R5 and C1 stabilize the 3.3V and 5V current limit loop. During a fault condition, R5 also serves to isolate C1 from the fast internal pull down resistor. Capacitors C7 and C8 are 0.01µF, per the CPCI

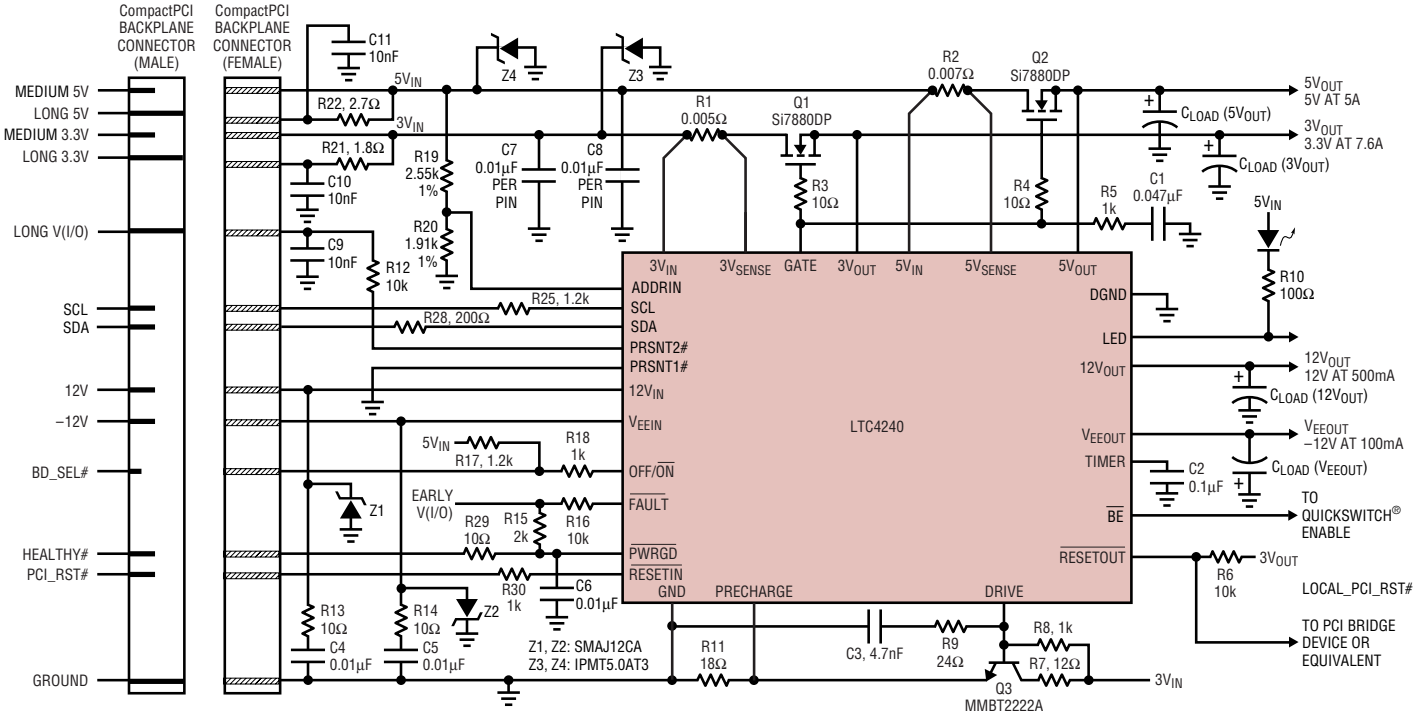


Figure 1. Typical CompactPCI application

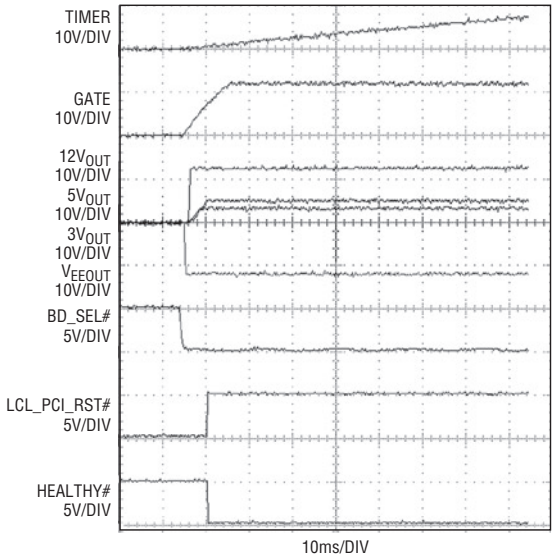


Figure 2. Typical power-up sequence

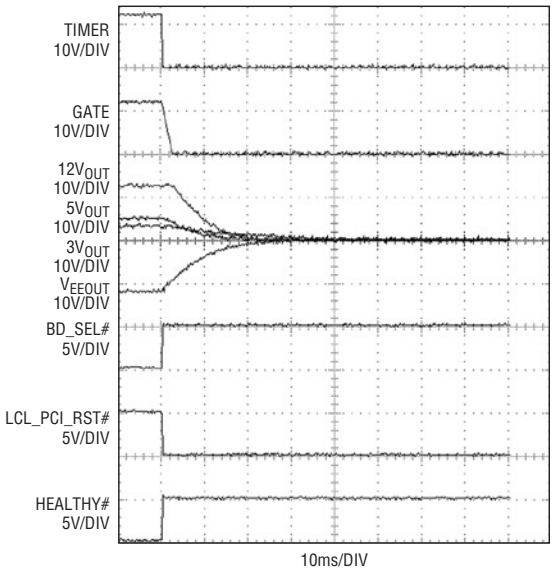


Figure 3. Power-down sequence

Hot Swap specification. On-chip power transistors isolate the –12V and +12V supplies. Transistor Q3 and its associated components form the pre-charge circuit.

CompactPCI Connection Pin Sequence

The staggered lengths of the CPCI male connector pins ensure that all power supplies are physically connected before back-end power is allowed to ramp (BD_SEL# asserted low). The long pins, which include 5V, 3.3V, V(I/O) and GND, mate first. The short pins, which includes BD_SEL# (OFF/$\overline{ON}$), mate last. The 3.3V and 5V long pins must be connected to the LTC4240 in order for the 1V PRECHARGE voltage to be available during early power. The following is a typical hot-plug sequence:

- ❑ ESD clips make contact.
- ❑ Long power and ground pins make contact and the 1V PRECHARGE becomes valid. Power is applied to the pull-up resistors connected to $\overline{FAULT}$, $\overline{PWRGD}$, and OFF/$\overline{ON}$ pins. The status LED is lit, indicating that the plug-in board is in the process of being connected (LOCAL_PCI_RST# is asserted). All power switches are off.
- ❑ Medium length pins make contact. There are six 5V and eight 3.3V medium length pins, bringing the 5V total to eight pins and the 3.3V total to ten pins. The CPCI specification limits the DC current to 1A/pin. The I^2C latch is initialized to allow seamless

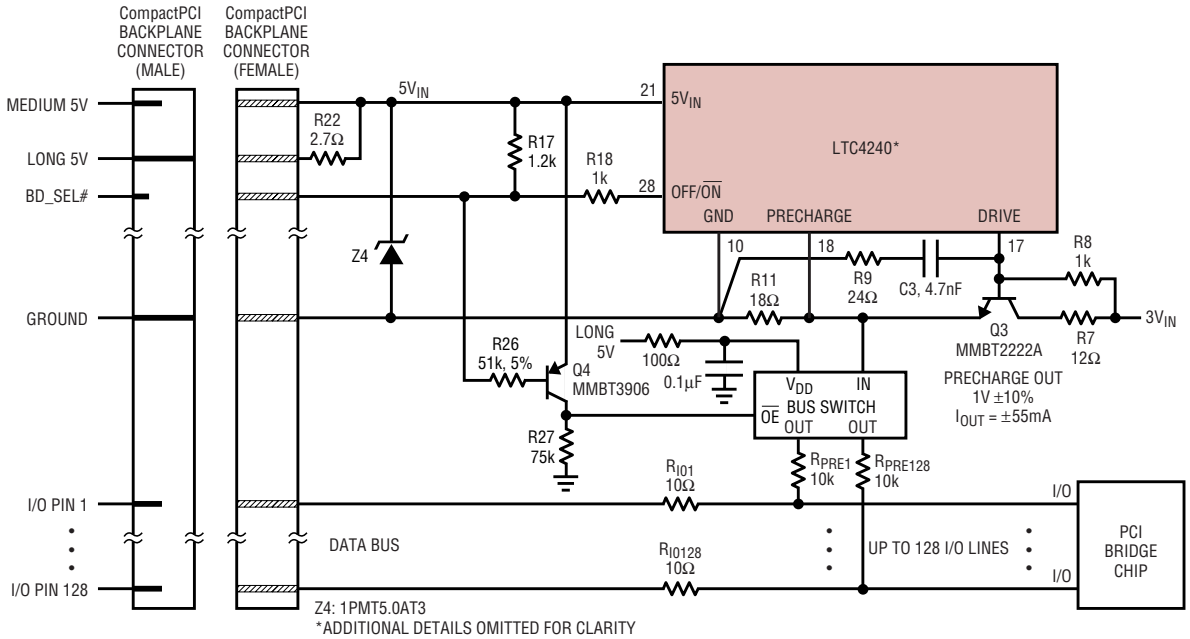


Figure 4. PRECHARGE bus switch application circuit for 3.3V and universal Hot Swap boards

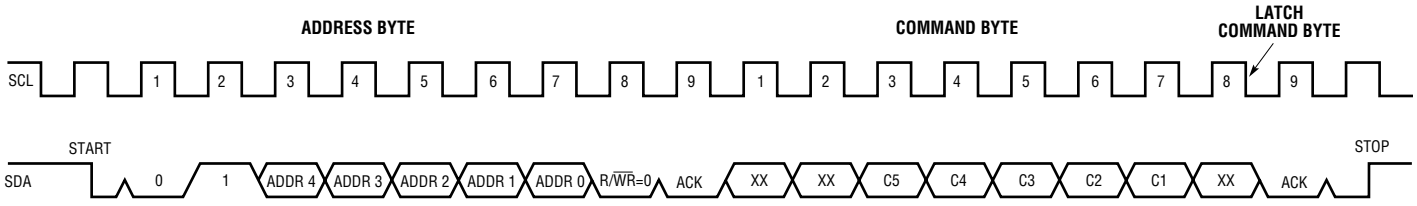
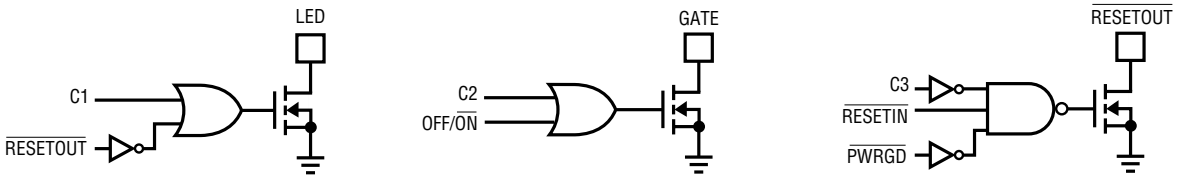


Figure 5. Send byte timing diagram



C1 TURNS ON THE EXTERNAL STATUS LED INDEPENDENT OF RESETOUT.

C2 PULLS DOWN THE GATE OF THE EXTERNAL N-CHANNEL SWITCHES. IT ALSO TURNS OFF THE $12V_{IN}$ AND V_{EEIN} INTERNAL POWER SWITCHES.

C3 IS USED TO SET LOCAL_PCI_RST# (RESETOUT).

Figure 6. Send byte command byte logic.

CPCI Hot Swap operation.

The +12V and –12V supply pins make contact at this stage. Zener clamps Z1 and Z2 plus shunt RC snubbers R13-C4 and R14-C5 help protect the +12V and –12V supply inputs, respectively, from large transient voltages during hot insertion and short circuit conditions. The signal pins also connect at this point. This includes the HEALTHY# signal connecting to the PWRGD pin, and the PCI_RST# signal connecting to the RESETIN pin.

- Short pins make contact last. BD_SEL# signal connects to the OFF/ON pin, thus starting the electrical connection process. If the BD_SEL# signal is grounded on the backplane, the electrical connection process begins immediately. The electrical connection process can be interrupted at any time via the I²C serial interface.

Power-Up Sequence

Figure 2 shows a typical power-up timing sequence. The connection sequence is triggered by a high to low transition on the BD_SEL# signal or by a power cycling executed by the I²C interface. A 65µA current source charges the gate nodes of the external power transistors. The power-up voltage rate of the 3VOUT and 5VOUT is approximately given by: dV/dt = 65µA/C1 or as determined by the current limit and the load capacitances.

Concurrently, an 11.5µA current source charges up the TIMER pin capacitance. Current limit faults are ignored until the voltage at the TIMER pin reaches 5.5V. Once all output supply voltages have crossed their power good thresholds, the HEALTHY# signal is pulled low (green LED turns on) and LOCAL_PCI_RST# is free to follow PCI_RST# and bit C3 of the I²C command latch.

Controlled Turn-Off Allows Safe Extraction

Figure 3 shows a typical power-down timing sequence. When either BD_SEL# or bit C2 of the I²C command latch is set high, a 200µA current source discharges the capacitance on the gates of the external FETs. The internal +12V and –12V power switches also turn off. The four power switches are turned off slowly to avoid glitching the power supplies. Internal resistors discharge the output load capacitors. Once the power-down sequence is complete, the status LED lights up and the CPCI card can then be safely removed from the slot.

Disconnecting PRECHARGE Resistors

Universal Hot Swap and 3.3V signaling boards use a 50k, or larger, resistor to precharge the I/O lines. Since leakage currents at the I/O lines can be as high as 10µA, a 10k biasing resistor is allowed, but must be disconnected during normal operation. Figure 4 shows an application circuit that connects the PRECHARGE voltage to the I/O lines during insertion, but disconnects the resistors once the BD_SEL# pin makes contact.

Table 1. Send byte definition

Bit	HIGH	LOW
C5	Ignore V_{EEOUT} Faults	Does not Ignore V_{EEOUT} Faults
C4	Ignore $12V_{OUT}$ Faults	Does not Ignore $12V_{OUT}$ Faults
C3	Sets RESETOUT Low	Does not Set RESETOUT Low
C2	Turns off all switches Overrides OFF/ON Pin	Does not turn off all switches Does not override OFF/ON pin
C1	Turns on LED	Does not turn on LED

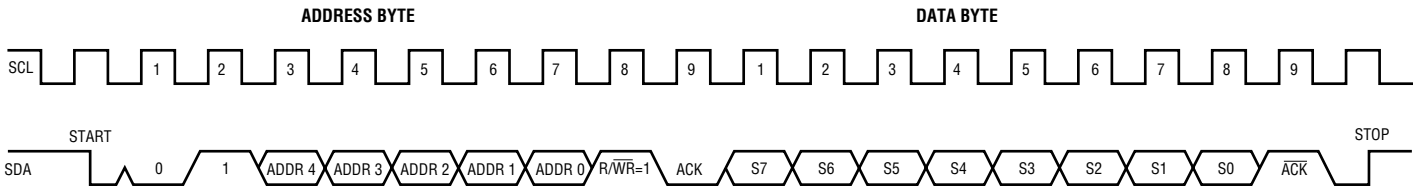


Figure 7. Receive byte timing

Table 2. Receive byte definition

S7	Logic State of the PRSNT2# Pin
S6	Logic State of the PRSNT1# Pin
S5	Logic State of the $\overline{\text{PWRGD}}$ Pin
S4	Logic State of the $\overline{\text{RESETOUT}}$ Pin
S3	Logic State of the $\overline{\text{RESETIN}}$ Pin
S2	FAULTCODE1 (See Table 3)
S1	FAULTCODE0 (See Table 3)
S0	Logic State of the $\overline{\text{FAULT}}$ pin

Table 3. Supply causing fault

FAULTCODE0	FAULTCODE1	$\overline{\text{FAULT}}$	Supply Causing Fault
LOW	LOW	LOW	$3V_{IN}$
LOW	HIGH	LOW	$5V_{IN}$
HIGH	LOW	LOW	$12V_{IN}$
HIGH	HIGH	LOW	V_{EEIN}
X	X	HIGH	None

Control and Monitor Card Power with I²C Interface

The LTC4240 incorporates an I²C compatible 2-wire (SCL, SDA) interface that allows the user to easily query and control the status of the LTC4240. A single analog pin selects 1 of 32 allowed addresses. The LTC4240 supports send byte and receive byte commands. Figure 5 and Table 1 depict the timing and bit definition of the send byte command. Figure 6 schematically outlines some of the command bit functions. Figure 7 shows the timing of the receive byte command. Tables 2 and 3 define the data byte. If a fault occurs, the FAULTCODE bits can be used to determine which supply generated the fault.

Conclusion

The LTC4240 provides a comprehensive solution to CompactPCI Hot Swap applications. An integrated I²C-compatible interface allows software control and monitoring of device function and power supply status. The LTC4240 control functions allow the plug-in board to be safely inserted or removed from a live CompactPCI slot without disturbing the system power supplies or I/O lines.

LTC3425, continued from page 5

size, 4.7µF ceramics, with a height of 1.35mm. Output voltage ripple is under $50mV_{P-P}$ at full load. The four low-cost inductors are only 1.55mm high, with a 3.2mm by 2.5mm footprint. The entire 5W power converter can fit into a 20mm by 16mm space, as seen in Figure 9.

2- or 3-Phase Operation

For cost-sensitive applications or for reduced board area with lower maximum current capability, the LTC3425 can be used as a 2- or 3-phase converter by simply de-populating one or two of the inductors. Figure 10 illustrates the typical efficiency difference between 2-, 3- and 4-phase operation. In Burst Mode, there is no efficiency penalty, since only phase A is used.

Conclusion: Good Things Do Come in Small Packages

The examples here illustrate the performance, flexibility, small size and ease-of-use of the LTC3425. The synchronous 4-phase architecture achieves high efficiency over a wide range of loads while enabling the use of low-profile components. The four-to-one reduction in output ripple current makes it possible to achieve very low output voltage ripple using small, lower cost ceramic capacitors. Users can choose between automatic or manual Burst Mode operation, pulse skipping mode or forced continuous conduction mode for noise sensitive applications. All these features, along with output disconnect, soft-start, 1µA shutdown current, anti-ringing control, thermal shutdown, a buffered reference output and a Power Good output are packed in a small 5mm by 5mm, thermally enhanced QFN package.

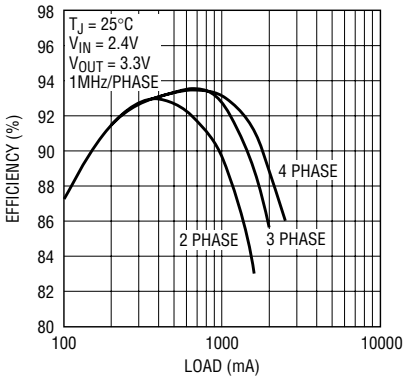


Figure 10. Typical efficiency with 2, 3 and 4 phases (fixed frequency mode)